Meddegamage Don Rangana Anton Malinda De Silva

Date of birth: 03/08/1993 | **Nationality:** Sri Lankan | **Gender:** Male |

(+94) 777398261 | ranganades@gmail.com | https://github.com/RanganaDe |

https://www.researchgate.net/profile/Rangana-De-Silva |

https://www.linkedin.com/in/rangana-de-silva/ |

Whatsapp Messenger: +94777398261 |

Silvereen, Padiwatte, Nattarampotha, 20194, Kandy, Sri Lanka

About me:
I am a software developer with 3+ years of work experience in the industry with acclaimed success in Java/J2EE development and in all phases of the Software development lifecycle. I see myself as a very enthusiastic person who would do something with truly understanding the concepts whilst being a good team worker.

TECHNICAL SKILLS

Technologies

- Java, J2EE, JPA
- MYSQL
- HTML, CSS
- Spring, JPA/Hibernate
- Maven, Jenkins, IntelliJ, Git

WORK EXPERIENCE

01/08/2021 – CURRENT – Colombo, Sri Lanka
SENIOR SOFTWARE ENGINEER – ENACTOR LTD PVT

Currently functioning as the development lead of the "Fiscalisation" team.

- Supervise and lead the team.
- Develop Fiscal Software solutions for European countries: Ukraine, France, Turkey, Austria and, Slovakia
- Skills: RESTful WebServices · Object-Relational Mapping (ORM) · Mockito · Reflection · Java RMI · java.net · Unit Testing · JMX · Java Swing · JavaServer Faces (JSF) · JSP · Spring Framework · Core Java

24/06/2019 – 01/08/2021 – Colombo, Sri Lanka
SOFTWARE ENGINEER – ENACTOR LTD PVT

The Main company product is a POS (Point of Sale) system for retailers.

- Worked on platform fixes and features for the Enactor Point of Sales System. [3 months]
- Joined the "Fiscalisation" team. The main vision of my team is to abide by government fiscal regulations and make sure retailers/government will operate without tax fraudulent or evasive activities.
- Develop Fiscal Software solutions for European countries: Hungary, Slovenia, Croatia, Germany, Romania, and Portugal
- Skills: Java Swing · Java, Cucumber, XML, Enactor Tool

01/11/2017 – 16/03/2018 – Espoo, Finland
UNIVERSITY RESEARCH ASSISTANT – AALTO UNIVERSITY

- Engaged in hardware simulation and troubleshooting critical issues to obtain accurate benchmark results for the technical paper.
- Systematic testing on the "dopserve" sample program whilst identifying a number of corner cases that require enhancements to the GCC-Plugin.
- Contributed to the research paper which was duly acknowledged.

EDUCATION AND TRAINING

25/11/2014 – 15/02/2019 – Peradeniya, Sri Lanka, Peradeniya, Sri Lanka
BACHELOR OF SCIENCE OF ENGINEERING SPECIALIZED IN COMPUTER ENGINEERING – University of Peradeniya

Field(s) of study

- Computer Engineering

3.35/4.00 GPA | https://eng.pdn.ac.lk/

01/2018 – 03/2018 – Otaneimi, Espoo, Espoo, Finland
MOBILE SYSTEM SECURITY COURSE – aalto university

4.0/5.0 GPA | https://ssg.aalto.fi/

DIGITAL SKILLS

My Digital Skills

- Information processing | Communication skills (listening skills; verbal skills; written skills) | Content creation | Problem Analysis & Problem Solving | Team-work oriented | Critical thinking

PUBLICATIONS

Hardware-based virus scanning acceleration

https://theiet.lk/wp-content/uploads/2017/10/24-p1.pdf – 2017
Rangana De Silva, Iranga Navaratna, Malitha Kumarasiri, and Hasindu Gamaarachchi, “Hardware-based virus scanning acceleration”, Present Around the World Competition and Annual Technical Conference 2017 organized by IET Sri Lanka.

On Power Analysis Attacks on Hardware Stream Ciphers

DOI: 10.1504/IJICS.2019.10023739
https://www.researchgate.net/publication/335667717_On_Power_Analysis_Attacks_against_Hardware_Stream_Ciphers – 2018
Rangana De Silva, Iranga Navaratna, Malitha Kumarasiri, Janaka Alawathugoda and Chai Wen Chauh “On Power Analysis Attacks on Hardware Stream Ciphers”, International Journal of Information and Computer Security (IJICS)

Correlation Power Analysis Attack on Software Implementation of TRIVIUM Stream Cipher

2021
Rangana De Silva, Iranga Navaratna, Malitha Kumarasiri, Janaka
Alawathugoda and Chai Wen Chauh “Correlation Power Analysis Attack on Software Implementation of TRIVIUM Stream Cipher”, International Journal of Information
and Computer Security (IJICS) [Under Review]

HardScope: Thwarting DOP attacks with Hardware-assisted Run-time Scope Enforcement

https://arxiv.org/pdf/1705.10295.pdf
Contributed to the research paper in my internship period at Aalto University, and was acknowledged for the work carried out.

PROJECTS

11/2016 – 12/2016
Hardware-Based Virus Scanning Acceleration

Special instructions along with respective hardware were added to support hardware-based virus scanning. An existing base processor was extended by adding special instructions and hardware units to accelerate virus scanning. The base processor was in Verilog. Testing was done on a Field programmable Gate Array (FPGA).
•Technologies: Verilog, FPGA, Altera Quartus
•Contribution: Extending the Verilog implemented base processor with new special instructions and carrying out timing analysis in FPGA for new and old processor designs to track down performance enhancement.
•Achievements: A+ for CO227 Computer Engineering Project. Published in IET conference.

05/2018 – 02/2019
Power Analysis Attacks on Trivium Stream Cipher

Power analysis attack carried out to break the Trivium cipher which is mostly used in hardware-based encryptions.
•Technologies: C, PIC microcontrollers, CUDA
•Contribution: Trivium implementation and debugging, setting up the testbed and verifying the testbed by attacking AES.
•Achievements: Research paper under review at International Journal of Information
and Computer Security (IJICS)

11/2017 – 03/2018
HardScope: Thwarting DOP with Hardware-assisted Run-time Scope Enforcement

Built a custom processor to mitigate Data-Oriented Programming attacks with runtime scope enforcement.
•Technologies: Verilog, Make, C, C++, Xilinx Vivado
•Contribution: Ran Software Simulated Processor on a configured Zed Board. Obtained benchmark results and reported them in the technical paper.
•Achievements: Contributed to the research paper which was duly acknowledged.

05/2017 – 10/2017
Contributed to OpenMRS

OpenMRS is a patient-based medical record system focusing on giving providers a free customizable electronic medical record system (EMR).

•Technologies: Java
•Contribution: bug fix on TRUNK-5047, New issue ticket TRUNK-5212

HONOURS AND AWARDS

17/10/2018

Information Security Quiz by CERT|CC Sri Lanka (4th Place) – CERT|CC Sri Lanka

Cyber Security Week 2018 was the annual National Conference in Cyber Security in Sri Lanka.

08/2017

"Hardware Based Virus Scanning Acceleration" paper Published and presented at the 24th Annual Conference of the IET Sri Lanka Network – IET Sri Lanka Network

Published the paper "Hardware Based Virus Scanning Acceleration in this conference and presented it.

08/2017

Present Around The World South Asian Regional Finals (Represented Sri lanka) – IET PATW Bangalore

07/2017

Best Presenter in IET Present Around The World Local Conference 2017 – IET Sri Lanka Network

2017

Community Judge at the Junction Hackathon, Finland

https://www.hackjunction.com/

COMMUNICATION AND INTERPERSONAL SKILLS

Best presenter in IET PATW local conference 2017

Skills gained by presenting research work.

Most popular idea award in Aces Hackathon 2016

Effective product marketing skills through communication

Demonstration of final year research project at Techno 2018

Sharing of technical information to non-technical groups

LANGUAGE SKILLS

Mother tongue(s): **SINHALESE**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	C1	B2	C1	C1	B2

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

LANGUAGE TEST RESULTS

23/10/2021

IELTS

- Candidate Number - 000897
- Test Report Form Numer 21LK000897DEM011A
- CEFR Level - C1